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Reduction of Lattice Thermal Conductivity in Single Bi-Te Core/Shell Nanowires with Rough Interface

*Joohoon Kang, Jong Wook Roh, Wooyoung Shim, Jinhee Ham, Jin-Seo Noh, and Wooyoung Lee**

Reducing the thermal conductivity of nanometer-scale materials is of significant interest for a broad range of applications in the dissipation of heat from electronics and optoelectronics, and in thermoelectric energy conversion. When the relevant length scale of a nanostructure is comparable to the mean free path of the heat carriers, the heat transport can be effectively controlled, which often results in the reduction of the thermal conductivity of the nanostructure compared to its bulk counterpart. The reduced thermal conductivity provides an effective strategy for optimizing thermoelectric energy conversion as well as for managing heat generated in electronic and photonic devices.

Considerable effort has been invested in developing methods to reduce thermal conductivity, largely because the reduction of thermal conductivity helps increase the thermoelectric figure-of-merit (ZT) (defined as $ZT = S^2\sigma T/\kappa$, where S, σ, κ, and T are the Seebeck coefficient, electrical conductivity, thermal conductivity, and absolute temperature, respectively).[1] In this respect, rational synthetic routes for κ reduction include the insertion of nanometer scale inclusions in bulk materials,[2] the epitaxial growth of superlattice thin films,[3] one-dimensional heterostructures,[4,5] and the use of photonic nanomesh structures.[6,7] A particularly versatile technique is to introduce a rough surface on silicon nanowires,[8] which provides efficient scattering across the broad phonon spectrum, and thus reduces κ as much as two orders of magnitude relative to bulk crystalline silicon. In a core/shell structure, which is low-dimensional heterostructures, has the significant advantage in the enhancement of ZT owing to low thermal conductivity by interface phonon scattering.[4,5] These strategies seem to be valid for a different material with phonons with a relatively long mean free path that is easily affected by the incorporation of phonon-scattering elements at comparble length scales. Here, we show that by using rough interface bismuth (Bi) –tellurium (Te) core/shell nanowires, we can reduce the thermal conductivity to 0.43 W/m·K, which is close to the amophous limit (~0.34 W/m·K), providing a route towards achieving low-κ materials. We find that the reduction in κ can be attributed to the rough interface acting as a secondary scattering phase, rather than to classical size effects.

Bi was chosen as the core material in the core/shell nanowire because of its potential for thermoelectric properties owing to a small effective mass (0.001 m_e), large thermoelectric power (50 to 100 μV/K), and small thermal conductivity (8 W/m·K), all of which help increase the thermoelectric figure-of-merit (ZT).[1] Bi-Te core/shell nanowires are prepared by the on-film formation of nanowires (OFF-ON) method,[9,10] which is capable of growing high-quality single-crystalline nanowires, and by the subsequent sputtering of Te onto the Bi nanowires. Taking advantage of the defect-free, highly crystalline Bi nanowire growth capability of the OFF-ON method,[11,12] we can focus only on the difference in the thermal conductivity between rough and smooth interface core/shell nanowires without unintended scattering caused by crystal defects.

To begin, Bi nanowires were prepared by the OFF-ON method with diameter and length of tens of nanometers and hundreds of micrometers, respectively (**Figure 1**). In a typical experiment, the as-deposited Bi films on a SiO_2/Si substrate are placed into a quartz tube and annealed at 260–270 °C, which induces compressive thermal stress in the Bi films due to the difference in thermal expansion between the Bi film and the SiO_2/Si substrate.[9,10,13] This compressive stress is the driving force that produces the Bi nanowires as a means of relieving the compressive stress. For smooth interface (SI) core-shell nanowire growth, the substrates on which the Bi nanowires have grown is cooled with liquid N_2, followed by Te deposition by radio frequency (rf) sputtering with a power of 12 W. Liquid N_2 cooling system and low sputtering power can minimize roughness on the surface of Bi nanowires due to suppressed kinetic energy of Te atoms. For rough interface (RI) core-shell nanowire growth, no substrate cooling was used, but Te deposition was done with a power of 30 W under ultra-high vacuum (UHV) conditions (refer to the Experimental Section for details), which helps physically etch the Bi nanowire surface.

The Bi-Te core/shell nanowries synthesized by this approach were confirmed with a cross-sectional scanning electron microscopy (SEM) (**Figure 2**a). The exposure of a suface to energetic particles, i.e. atom bombardment during Te sputtering, can change Bi nanowire surface morphology.[14] High-power Te sputtering onto Bi nanowires is expected to have similar effects. The surface morphology change by incident Te atoms is not likely to be uniform at the nanometer scale, and as a consequence, causes rough surfaces at a comparable length scale.[15,16] Transmission electron microscopy (TEM) shows the

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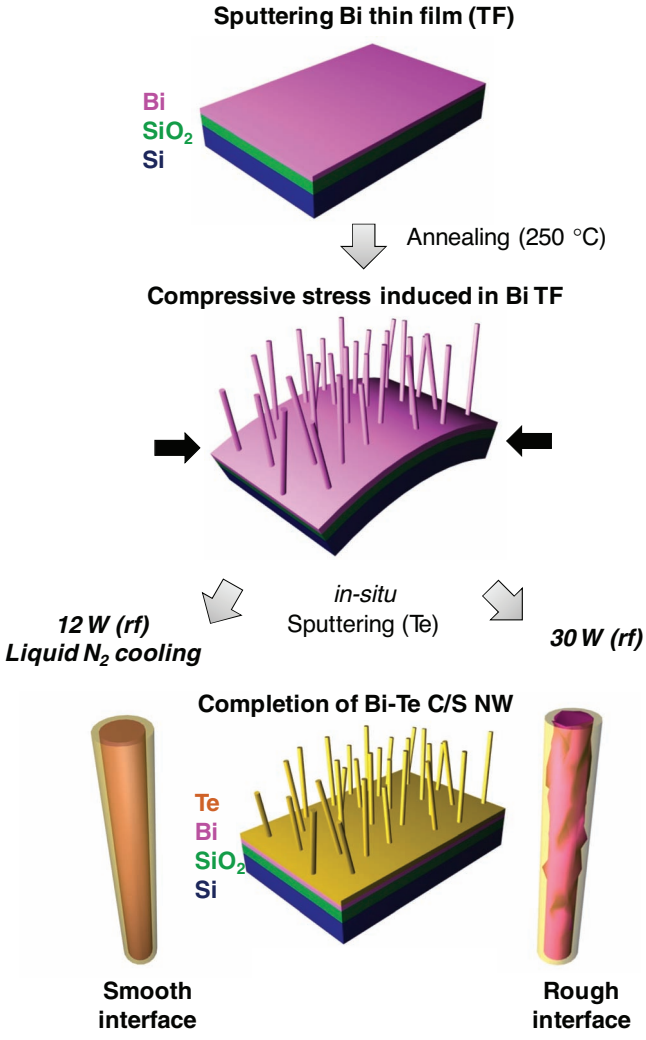

Figure 1. Schematic representations of Bi-Te core/shell nanowire growth based on the OFF-ON method. (Step 1) A Bi thin film is deposited onto the oxidized Si substrate using UHV RF sputtering. (Step 2) During annealing at 260–270 °C for 10 h, a compressive stress is induced in the Bi film. Bi nanowires are grown from the Bi film to release the stored compressive stress. (Step 3) A Te thin film is deposited onto the substrate containing the Bi nanowires using UHV RF sputtering. For smooth interface core-shell nanowire growth, the substrates where Bi nanowires have grown are cooled with liquid N_2, followed by Te deposition by RF sputtering with a power of 12 W (left). For rough interface core-shell nanowire growth, no substrate cooling was used, but Te deposition was done with power of 30 W under UHV conditions (right). A magnified view of an individual Bi-Te core/shell nanowire is also presented.

interface of the nanowire, which confirms the presence of the rough interface generated by Te deposition at relatively high power, whereas a Te shell deposited at low power produces a smooth interface (Figure 2b). The mean roughness at the rough interfaces of the core-shell nanowires varied from wire to wire, but was typically 5–10 nm with a roughness period of the order of several nanometers. From a high-resolution transmission electron microscopy (HR-TEM) image of a cross-section of a RI core/shell nanowire (Figure 2c), the existence of the rough

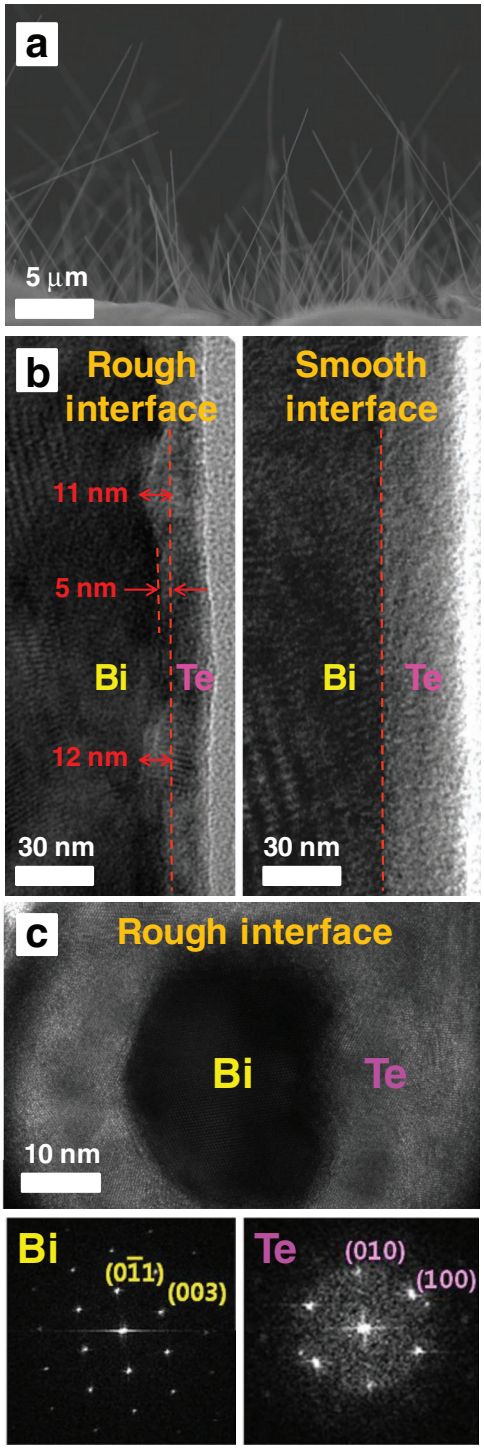

Figure 2. Electron microscopy images of the Bi-Te core/shell nanowires. (a) SEM image of the Bi-Te core/shell nanowires. (b) Low magnification TEM image of an individual Bi-Te core/shell nanowire. The presence of the rough interface (mean roughness height: 5–10 nm) generated by Te deposition at relatively high power (left), whereas a low power for depositing Te shell produces smooth interface (right) (c) High resolution cross-sectional TEM image of a Bi-Te core/shell nanowire. Bottom images show SAED patterns of the Bi core and the Te shell.

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surface is clearly seen. Selected area electron diffraction (SAED) patterns reveal that the sputtered Te shell exhibits a low degree of crystallinity or a quasi-amorphous surface, while the Bi core is highly single-crystalline.

The chemical composition of the Bi-Te core/shell nanowire was also confirmed by energy dispersive X-ray spectroscopy (EDS). **Figure 3**a is a scanning TEM (STEM) image of the cross-section of a RI core/shell nanowire with a Pt coating. The EDS line scan profile revealed the spatial distribution of Bi and Te at the core and shell, respectively, which is further confirmed by STEM elemental mapping images across the same cross-sectional area (Figure 3b and c). EDS scanning experiments at arbitrary positions on the nanowire not only quantitatively confirm that the Bi core and Te shell are present, but also support the claim that the formation of a Bi_xTe_{1-x} compound nanowire can be ruled out.

We performed thermal conductivity measurements on the individual Bi-Te core/shell nanowires. In order to measure the thermal conductivity of an individual Bi-Te core/shell nanowire without thermal conduction through a substrate, we utilized suspended micro-electro-mechanical system (MEMS) devices.[17,18] **Figure 4**a shows a SEM image of a suspended MEMS device that consists of two silicon nitride (SiNx) membranes supported by five long beams. A Bi-Te core/shell nanowire was placed between the two suspended membranes by a drop-casting method.[17] Then, to improve thermal contact between the Bi-Te core/shell nanowire and the membranes, a Pt/C composite was locally deposited using a dual-beam focused ion beam (FIB) (inset of Figure 4a). With negligible radiation loss, the Bi-Te core/shell nanowire should be the only path to conduct heat between the heating membrane and the sensing membrane. The thermal contact resistance was found to be negligible, from a duplicated contact experiment, which revealed that thermal conductivity remained unchanged even after the second thermal contact was made in the vicinity of the first one (see Supporting Information, Figure S3). Under these conditions, the thermal conductivity of a Bi-Te core/shell nanowire was calculated from the measured thermal conductance, which was determined from temparature changes in the heating and sensing membranes. The detailed method for calculating the thermal conductivity of a nanowire is explained in the previous studies.[17,18]

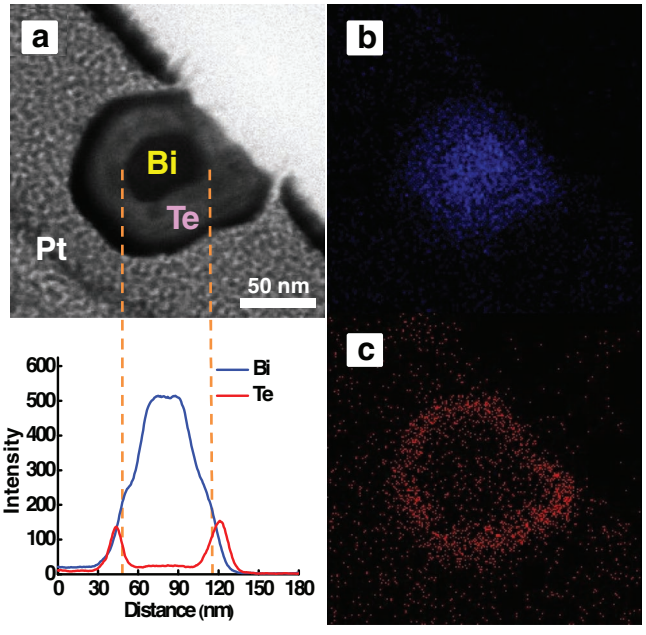

Figure 3. Spatial distribution of elements over the cross-section of a Bi-Te core/shell nanowire. (a) Scanning TEM (STEM) image of a Bi-Te core/shell nanowire. The EDX line profiles indicate the core/shell structure consisting of a Bi core (blue line) and Te shell (red line). (b), (c) Element maps also show Bi core (blue dots) and Te shell (red dots) regions in the nanowire.

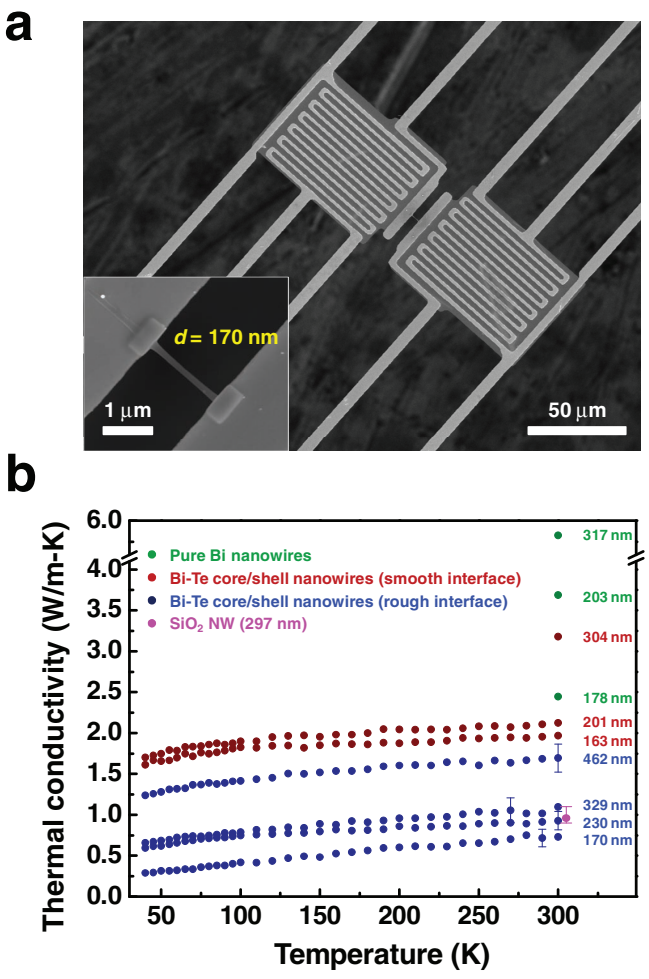

Figure 4. MEMS device and thermal conductivities of the Bi-Te core/shell nanowires. (a) SEM image of a suspended MEMS device for measuring the thermal conductivity of an individual Bi-Te core/shell nanowire. The individual Bi-Te core/shell nanowire is placed between two membranes. Pt/C composite is locally deposited to improve the thermal contacts between the nanowire and membranes using a dual-beam focused ion beam (inset). (b) The thermal conductivities of the pure Bi nanowires, the RI Bi-Te core/shell nanowires with d = 170, 230, 329, and 462 nm, and the SI Bi-Te core/shell nanowires with d = 163, 201, and 304 nm measured in the temperature range of 40 to 300 K. See methods for error determination of thermal conductivity at 300 K. κ of a SiO_2 nanowire at 300 K is also indicated and compared to a literature value[19] to confirm the reliability of the measurement.

The thermal conductivity, κ_{total}, values for individual RI Bi-Te core/shell nanowires with different diameters as a function of temperature (in comparison to smooth interface Bi-Te core/shell and pure Bi nanowires) are shown in Figure 4b. The room temperature κ of a SiO_2 nanowire is also measured and compared to a literature value[19] in order to confirm the reliability of the measurements (see Supporting Information, Figure S2 for details). The experimental errors are indicated at room temperature, and are associated with noise arising from the electrical measurements and inaccuracies in the measurement of the nanowire area by SEM. For comparison, specific diameters of SI core/shell nanowires (163 nm, 201 nm, and 304 nm) and pure Bi nanowires (178 nm, 203 nm, and 317 nm) were chosen, which are comparable to the diameters of the RI core/shell nanowires (170 nm, 230 nm, and 329 nm). We found that the κ_{total} of all nanowires is strongly diameter-dependent, which is attributed to the classical size effect. An interesting general trend for measured κ_{total} is that the κ_{total} values of RI core-shell nanowires is two- and fivefold times lower than κ_{total} for SI core-shell and pure nanowires of comparable diameters, respectively. For example, measured κ_{total} of 1.97 W/m·K (163 nm), 2.12 W/m·K (201 nm), and 3.18 W/m·K (304 nm) in SI core-shell nanowires were larger than measured κ_{total} values of 0.73 W/m·K (163 nm), 0.93 W/m·K (201 nm), and 1.10 W/m·K (304 nm) in RI core-shell nanowires. Because few nanometer surface roughness barely changes electrical resistance, there is no significant resistivity change between SI and RI core-shell nanowires (see Supporting Information, Table S1). Based on this observation, the reduction of κ_{total} can be attributed to the reduction of the lattice thermal conductivity (κ_L) rather than the electronic thermal conductivity (κ_E).

κ_L for the 170-nm RI core-shell nanowire, for example, was obtained by subtracting κ_E, which can be calculated using the Wiedemann-Franz law, $\kappa_E = L\sigma T$, where L is the Lorenz number, σ is the electrical conductivity and T is the absolute temperature. The Lorenz number for a degenerate system corresponds to 2.44×10^{-8} W·Ω/K^2, and for most conductors it is between 2.2 and 2.7×10^{-8} W·Ω/K^2.[20] Recent studies show that the Lorenz number of a 1D metal nanowire is found to be smaller than its bulk counterpart[21] and is also reduced with a decrease in carrier concentration that increases resistivity.[22] In this sense, our nanowires, which are 1D systems and have a higher resistivity than the bulk counterparts, are likely to have a lower Lorenz number than the bulk. For this reason, we have chosen the lower limit of the Lorenz number, 2.2×10^{-8} W·Ω/K^2, since the measured resistivity of the nanowires (1D system) in this study (10^{-3}–10^{-4} Ω·cm) is larger than that of bulk Bi (10^{-5}). In fact, this lower limit (2.2×10^{-8} W·Ω/K^2) has been used in doped Si nanowires with a 1.7×10^{-3} Ω·cm resistivity to calculate the lattice thermal conductivity.[8] With measured κ_{total} and σ for 170 nm RI core/shell nanowire at room temperature, κ_L is 0.43 W/m·K, which is close to the κ_L of bismuth oxide (0.34 W/m·K).[23] This value is four times lower than the κ_L of 163-nm SI core-shell nanowire (1.62 W/m·K). It is worth noting that κ_E for RI (0.32 W/m·K) and SI (0.35 W/m·K) core/shell nanowires are almost identical. It is now clear that a large decrease in lattice thermal conductivity occurs with rough interfaces. All measured κ_{total}, ρ ($1/\sigma$) and calculated κ_E and κ_L for nanowires of different diameters are summarized in Table S1 in the Supporting Information.

In **Figure 5**a, we further compare the temperature dependent κ at low temperatures (30–70 K), and a clear trend for the temperature power rule (T^3 for bulk) is also observed, which indicates that specific scattering effect is decreasing the temperature power to ~0.1 for the RI 170-nm Bi-Te core/shell nanowire. This implies that the rough interface, rather than wire boundary, may be the dominant scattering phase that reduces κ in the Bi-Te core/shell nanowires. In addtion, the κ_{total} values for nanowires as a function of diameter at room temperature are shown in Figure 5b. In the case of the RI core-shell nanowires (blue symbols), κ_{total} variation over diameter change ($\Delta\kappa/\Delta d$) is merely 0.003 [w/m·K]/nm, which is smaller than that of the pure Bi nanowires (green symbols: 0.016 [w/m·K]/nm) or the

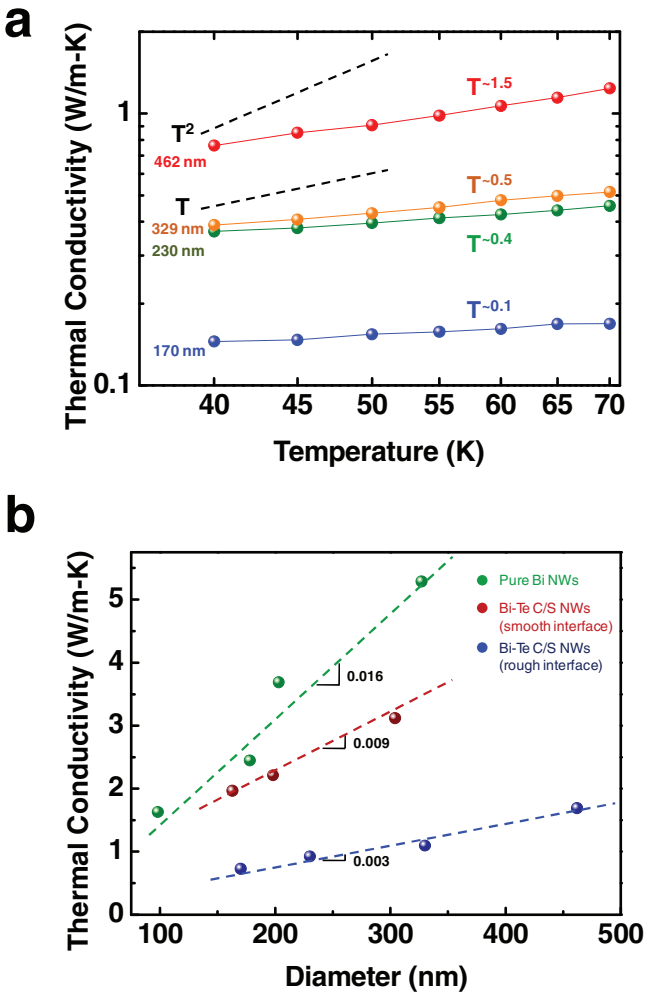

Figure 5. Low temperature and diameter dependence of thermal conductivity. (a) Low temperature dependence of thermal conductivities of RI core/shell nanowire on a logarithmic scale with T^1 and T^2. (b) Comparison of diameter-dependent thermal conductivities between the measured values of pure Bi nanowires (green symbols), the Bi-Te core/shell nanowires with a smooth interface (red symbols), and the Bi-Te core/shell nanowires with a rough interface (blue symbols). κ_{total} variation over diameter changes ($\Delta\kappa/\Delta d$) in the RI core/shell nanowires is 0.003 [w/m·K]/nm, which is smaller than those of the pure Bi nanowires (0.016 [w/m·K]/nm) or the SI core/shell nanowires (0.009 [w/m·K]/nm).

SI core/shell nanowires (red symbols: 0.009 [w/m·K]/nm). This indicates that the influence of the rough interface is sufficient to dominate the nanowire size effects that are relevant to wire boundary scattering of phonons. Introducing scattering at additional length scales rather than the nanowire diameter further reduces the thermal conductivity, and a system whose mean free path for phonons is longer than that of charge carriers takes advantage of this strategy.[8] For Bi, the mean free path of electrons and holes (without an applied electric field) is estimated to be ~100 nm at room temperature,[24] whereas the mean free path for phonons at room temperature is unclear, e.g. ~150 nm[25] and 11 nm based on the empirical relation.[26] A study of Bi thin film suggests that phonons may have a longer mean free path than electrons in Bi.[26,27] Based upon our experimental results, where phonons are effectively suppressed, we propose that the phonon mean free path in the studied nanowires may be longer than the electron mean free path. Consequently, the rough interface plays a pivotal role in suppressing phonon transport, which in turn, reduces thermal conductivity significantly.

In conclusion, we have investigated the reduction of the lattice thermal conductivity of Bi-Te core/shell nanowires with rough interfaces. A combination of the OFF-ON method and sputtering yields core/shell nanowires with single-crystalline Bi cores and Te shells with a rough interface in between. The thermal conductivity measured for a rough interface Bi-Te core/shell nanowire was smaller than that of a smooth interface Bi nanowire. From these results, it is proposed that the rough interface effectively suppresses phonon contribution to thermal conductivity. Although the values of κ_E and κ_L calculated from measured κ_{total} and ρ may not be precisely correct because the exact Lorenz number is unknown, a qualitative trend of the thermal conductivity reduction in RI core/shell nanowires compared to SI core/shell nanowires demonstrates at least that low-κ can be achieved by this route. Moving forward, an exact mechanism for such thermal conductivity reduction needs to be identified to fully exploit the advantage afforded by this approach.

Experimental Section

Nanowire growth: The Bi-Te core/shell nanowires were fabricated by the combined use of the on-film formation of nanowires (OFF-ON) method and a simple sputtering technique. First, Bi nanowires were grown from a Bi thin film using the OFF-ON method, which is a spontaneous nanowire growth technique based on the compressive stress arising from the large difference in thermal expansion coefficients of a Bi film (13.4×10^{-6} °C) and the SiO_2/Si substrate ((0.5×10^{-6} °C)/(2.4×10^{-6} °C)). The Bi thin film was initially deposited onto a thermally oxidized Si (100) substrate at a rate of 32.7 Å/s by radio frequency (rf) magnetron sputtering under a base pressure of 4×10^{-8} Torr. During this Bi thin film deposition, the substrate was kept cool using liquid nitrogen to achieve the small grain morphology that would lead to small-diameter Bi nanowires in the following step. The Bi film subsequently underwent thermal annealing at 260 to 270 °C for 10 h to drive the Bi nanowire growth.[9,10] Once the OFF-ON process was completed, a 30-nm thick Te film was deposited in situ onto the Bi nanowires at room temperature, using rf magnetron sputtering. For smooth interface (SI) core-shell nanowire growth, the substrate where Bi nanowires have grown are cooled with liquid N_2, followed by Te depostion by rf sputtering with a power of 12 W. For rough interface (RI) core-shell nanowire growth, no substrate cooling was used, but Te deposition was done with power of 30 W under ultra-high vacuum (UHV) conditions.

Thermal conductivity measurement: Thermal conductivity measurements on the individual nanowires were performed using the MEMS device shown in Figure 4a. A direct current (DC) voltage applied to the Pt coil on the heating membrane generates Joule heat, which increases the temperature of the heating membrane (T_h). The temperature is converted from the resistance of the Pt coil on the heating membrane (R_h), which is measured by four-point electrodes connected to the Pt coil. A certain amount of heat generated by the Pt coil on the heating membrane is conducted to the sensing membrane through an individual Bi-Te core/shell nanowire under a thermal steady state condition. Due to the thermal conductance through the Bi-Te core/shell nanowire (G_w), the temperature of the sensing membrane (T_s) is also increased, as is the resistance of the Pt coil on the sensing membrane (R_s). The thermal conductance of a Bi-Te core/shell nanowire (G_w) can be obtained from the following equation: $G_w = [P/(\Delta T_h - \Delta T_s)] \times [(\Delta T_s)/(\Delta T_h + \Delta T_s)]$, where $P = I^2 \times [(R_h + R_l)/2]$ and R_l is the total lead resistance of the Pt lines that connect to the Pt coil on the heating membrane. The thermal conductivity (κ) is calculated from a measured G_w, using $\kappa = (G_w L)/A$, where L is the length between the thermal contacts and A is the cross-sectional area of a nanowire.[17]

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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